IN THE ABSTRACT

In ~~a~~ an insulated double gate FET, the threshold voltage during the operation of a transient response thereof is enabled to be arbitrarily and accurately controlled by a method that includes applying a first input signal intended to perform an ordinary logic operation to one of the gate electrodes thereof and applying, in response to this signal, a second signal that has a signal-level temporal-change direction as the first input signal and has at least one of the low level and the high level thereof shifted by a predetermined magnitude or endowed with a predetermined time difference or has the time slower or faster signal level change of the signal to the other gate electrode.

Please replace paragraph [0001] with the following rewritten paragraph:

This invention relates to a method for the application of a gating signal in [[a]] an insulated double gate field effect transistor (FET).

Please replace paragraph [0003] with the following rewritten paragraph:

As one of the element configurations directed toward this prevention, [[a]] an insulated double gate FET illustrated in FIG. 1 may be adduced, for example (Japanese Patent No. 2021931). In the diagram, 1 denotes a substrate, 2 a second gate insulating film concurrently serving as an insulating layer for separating a semiconductor crystal layer formed on the substrate from the substrate, though not wholly illustrated, 3, 4 and 5 respectively a source region, a drain region and a channel region formed in part of the semiconductor crystal layer, 6 a first gate insulating film, 7 an insulating film, 8 a source electrode, 9 a drain electrode, 10 a first gate electrode, and 11 a second gate electrode.

Please replace paragraph [0006] with the following rewritten paragraph:

The insulated double gate FET can avoid this problem because it is capable of using a channel region of an extremely low concentration approximating an intrinsic semiconductor without impairing the restriction of the short channel effect. For the purpose of realizing a right threshold voltage, it is inevitable to use a metal possessing an appropriate work function as the material for the gate electrode. The metal, however, allows no fine control of the work function because the work function has a discrete value for metal to metal. A method that attempts to produce a material manifesting a proper work function by using SiGe, for example, and properly selecting the ratio of Si and Ge has been proposed. This method, however, is at a disadvantage in complicating the process to be used for the production.

Please replace paragraph [0007] with the following rewritten paragraph:

The preceding description has depicted the insulated double gate FET as having the two gates thereof electrically connected to each other. There has been known a method which comprises using one of the gate electrodes for signal input and applying to the other gate electrode a stated constant potential (though the magnitude of the constant potential varies at any time, there are times when the potential may be retained at least at a fixed magnitude during a period amply longer than the cycle of input signal) as illustrated in FIG. 2(d), thereby controlling the threshold voltage seen from the signal input gate at the optimum magnitude. Since the electric current flows only through the channel on the signal input gate side, this method is at a disadvantage in suffering the amount of electric current to be roughly halved from the amount obtained when the two gate electrodes are electrically connected and inducing a degradation of the load driving ability during the operation of transient response. It is further at a disadvantage in widening the so-called gate swing (otherwise called "S factor" and reported in the denomination of "mV/digit") so much as to pose an awful question as to how much change in gate voltage is necessary for shifting the drain current by one order of magnitude below the threshold voltage. Incidentally, when the two gate electrodes are electrically connected, such a small magnitude at room temperature as about 60 mV/decade that substantially approximates the theoretical limit is realized.

Please replace paragraph [0008] with the following rewritten paragraph:

This invention is directed toward providing a method for applying a gating signal in [[a]] an insulated double gate FET that eliminates the drawbacks mentioned above and enables the threshold voltage to be arbitrarily controlled with high accuracy.

Please replace paragraph [0009] with the following rewritten paragraph:

The method according to this invention for the application of a gating signal in [[a]] an insulated double gate FET comprises applying, in response to a first signal fed into a first gate electrode of the insulated double gate FET, to a second gate electrode a second signal that has a temporal change of a signal level in a same direction as the first signal and (i) has a signal level shifted by a predetermined magnitude or (ii) has a slower or faster rise time or a fall time or (iii) has admitted a predetermined time difference.

Please replace paragraph [0010] with the following rewritten paragraph:

This invention further embraces an integrated circuit that possesses [[a]] an insulated double gate FET using the aforementioned method for applying a gating signal.

Please replace paragraph [0011] with the following rewritten paragraph:

This invention, as described above, consists in enabling the threshold voltage of [[a]] an insulated double gate FET to be controlled arbitrarily with high accuracy by applying, in response to a first signal fed into a first gate electrode of the insulated double gate FET, to a second gate electrode a second signal which has a same direction of temporal change as the first signal and (i) has a signal level shifted by a predetermined magnitude or (ii) has a rise time or a fall time advanced or delayed or (iii) has admitted a predetermined time difference.

Please replace paragraph [0012] with the following rewritten paragraph:

FIG. 1 is a cross section illustrating one example of the conventional insulated double gate FET.

Please replace paragraph [0014] with the following rewritten paragraph:

FIG. 3 is a gate characteristic diagram of [[a]] an insulated double gate FET determined by the conventional method for applying a gate input.

Please replace paragraph [0015] with the following rewritten paragraph:

FIG. 4 is a gate characteristic diagram of [[a]] an insulated double gate FET determined by the method of this invention for applying a gate input.

Please replace paragraph [0016] with the following rewritten paragraph:

FIG. 5 is a gate characteristic diagram of [[a]] an insulated double gate FET determined by a method for applying a gating input when a delayed signal of this invention is applied.

Please replace paragraph [0017] with the following rewritten paragraph:

FIG. 6 illustrates graphic symbols used to represent [[a]] an insulated double gate FET in a circuit diagram, FIG. 6(a) depicting an n channel element and FIG. 6(b) a p channel element.

Please replace paragraph [0024] with the following rewritten paragraph:

The method for the application of a gating signal in [[a]] an insulated double gate FET according to this invention comprises applying an input signal for ordinary logical operation to one of the gate electrodes of the insulated double gate FET during the operation of transient response and applying to the other gate electrode a signal having a temporal change of a signal level in one and the same direction as the signal first mentioned above (hereinafter referred to "in-phase"), which (i) has at least one of the low level and the high level of the

signal shifted by a predetermined magnitude or (ii) has the slower or faster signal level change or (iii) has admitted a predetermined time difference (advance or delay).

Please replace paragraph [0026] with the following rewritten paragraph:

The case of the n-type FET will be explained below by way of illustration. As usual, an input signal Vg1 is applied to one of the gate electrodes of [[a]] an insulated double gate FET (the first gate, for example), and a voltage lower than the threshold voltage VT0 which exists when the two gate electrodes are mutually connected and operated, such as a constant voltage Vg2 that is -0.5 V or -1.0 V, for example, is applied at the same time to the other gate electrode (the second gate electrode, for example).

Please replace paragraph [0029] with the following rewritten paragraph:

In contrast, in the first method of this invention, an input signal Vg1 is applied to one of the gate electrodes of the insulated double gate FET (the first gate electrode, for example), and an input signal Vg2 resulting from shifting at least the low level of the Vgl by a lower voltage than the threshold voltage VT0 existing when the two gate electrodes are mutually connected and operated, such as -0.5 V (Vg1 - Vg2 = 0.5 V) or -1.0 V (Vg1 - Vg2 = 1.0 V), for example, is applied at the same time to the other gate electrode (the second gate electrode, for example), as shown in FIG. 2(a).

Please replace paragraph [0045] with the following rewritten paragraph:

For a start, FIG. 6 shows the graphic symbols of [[a]] an insulated double gate FET that are used in the circuit diagram. FIG. 6(a) represents an n channel element and FIG. 6(b) a p channel element. Then, 100 denotes a first gate electrode, 200 a second gate electrode, 300 a drain electrode, and 400 a source electrode.

Please replace paragraph [0051] with the following rewritten paragraph:

FIG. 12 illustrates a concrete embodiment of the third method of this invention applied to the inverter circuit of a double rail logic circuit. X1 and X2 each denote [[a]] an insulated double gate FET, and the second gate electrodes of X1 and X2 are respectively cross-linked to the drain electrodes of X2 and X1. Then, reference numerals 28 and 29 denote signal input terminals and numeral 30 and 31 denote output terminals. As logical values, these terminals emit mutually complementary values. Denoted by 32 is a VDD terminal of the drain power source, and by 33 is a VSS terminal of the source power source. This circuit functions as an inverter circuit for the so-called double rail logic circuit.

Please replace paragraph [0057] with the following rewritten paragraph:

The method according to this invention for the application of a gating electrode signal in [[a]] an insulated double gate FET is directed toward enabling the threshold of the insulated double gate FET to be controlled arbitrarily and accurately by applying, in response to a first signal fed into a first gate electrode, a second signal that has a same signal-level temporal-change direction as the first signal and (i) has a signal level shifted by a predetermined magnitude or (ii) has a slower or faster rise time or a fall time or (iii) has admitted a predetermined time difference to the second gate electrode.